Course Code: 19CS0504 **R19**

SIDDHARTH INSTITUTE OF ENGINEERING & TECHNOLOGY::PUTTUR
(AUTONOMOUS)
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QUESTION BANK (DESCRIPTIVE)

Subject with Code: Computer Organization & Architecture(19CS0504) **Course & Branch :** B.Tech - CSE
Year & Sem : II B.Tech & I-Sem **Regulation :** R19

UNIT –I

BASIC STRUCTURE OF COMPUTERS

1		Sketch the basic functional unit of computer and explain each unit in detail.	[L3][CO1]	**[12M]**
2	a	Discuss about Bus structure with neat sketch.	[L2][CO1]	**[08M]**
	b	Illustrate the types of Bus.	[L3][CO1]	**[04M]**
3	a	Explain the Instruction Cycle with neat diagram.	[L4][CO1]	**[06M]**
	b	Write in detail about the Basic Operational Concepts with neat diagram.	[L3][CO1]	**[06M]**
4	a	Identify various steps of instruction cycle?	[L2][CO1]	**[04M]**
	b	List out the Computer Instructions and Explain about it.	[L1,L3][CO1]	**[08M]**
5		Summarize the Addressing Modes with neat sketch.	[L5][CO1]	**[12M]**
6		Assess the Data Manipulation Instructions and their types.	[L5][CO1]	**[12M]**
7	a	Discuss about Program counter and Memory Address register.	[L2][CO1]	**[04M]**
	b	Explain in detail about Data Transfer Instructions?	[L2][CO1]	**[08M]**
8		Interpret Program Control Instructions.	[L3][CO1]	**[12M]**
9		Illustrate any four addressing modes with neat sketch.	[L3][CO1]	**[12M]**
10	a	Differentiate between I/O unit and memory Unit?	[L3][CO1]	**[04M]**
	b	Write a note on basic I/O operations.	[L3][CO1]	**[08M]**

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UNIT –II

DATA REPRESENTATION & COMPUTER ARITHMETIC

1		Develop a Flowchart and Algorithm for Add/Sub with an example.	[L3][CO2]	**[12M]**
2		Show the steps of signed operand multiplication with example?	[L2][CO2]	**[12M]**
3		Prepare a flowchart for Multiplication of positive numbers and steps with an example.	[L6][CO2]	**[12M]**
4	a	Compare signed number, 1's complement, 2's complement with an example.	[L5][CO2]	**[04M]**
	b	Describe about fixed and floating point representations.	[L2][CO2]	**[08M]**
5		Illustrate the steps in Booth multiplication algorithm and Draw the flowchart with an example.	[L3][CO2]	**[12M]**
6		Invent the steps of Division restoring and draw the flow chart with an example.	[L6][CO2]	**[12M]**
7		Prepare the Flowchart and write algorithm for Division non-restoring with an example.	[L3][CO2]	**[12M]**
8		Describe the Floating point numbers, its operations and implementation.	[L2][CO2]	**[12M]**
9		Explain about signed number and fixed point representations.	[L2][CO2]	**[12M]**
10		Show the step by step signed-operand multiplication process using Booth algorithm When (-9) and (-13) are multiplied. Assume 5-bit registers to hold signed numbers and (-9) to be the multiplicand.	[L4][CO2]	**[12M]**

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UNIT –III

REGISTER TRANSFER & MICRO OPERATIONS

1	a	Design the block diagram of the hardware that implements the following register transfer statement P: R2←R1.	[L6][CO3]	**[08M]**
	b	Construct a 4-line common bus system with a neat diagram.	[L6][CO3]	**[04M]**
2	a	Illustrate the three- state bus buffers with neat sketch.	[L3][CO3]	**[06M]**
	b	Write about binary increment with neat sketch.	[L4][CO3]	**[06M]**
3	a	Describe about 4-bit incrementar with suitable example?	[L2][CO3]	**[04M]**
	b	What is Hardwired Control? Explain in detail with a neat diagram.	[L4][CO3]	**[08M]**
4	Define register transfer language? Explain in detail.		[L4][CO3]	**[12M]**
5	Describe the Micro Programmed Control with a neat sketch.		[L2][CO3]	**[12M]**
6	Survey the Address Sequencing with neat diagram.		[L4][CO3]	**[12M]**
7	a	Examine the Bus transfer with neat diagram.	[L3][CO3]	**[06M]**
	b	Summarize the Register Representations and way it is used.	[L5][CO3]	**[06M]**
8	Explain in detail about Arithmetic Micro Operations?		[L3][CO3]	**[12M]**
9	Write in detail about Logic Micro Operations with neat representations?		[L3][CO3]	**[12M]**
10	Explain shift micro operations and draw 4 bit combinational circuit shifter.		[L4][CO3]	**[12M]**

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UNIT –IV

MEMORY ORGANIZATION

1	a	Assess the Memory Hierarchy with neat sketch	[L5][CO4]	**[08M]**
	b	Discuss briefly about synchronous DRAMs?	[L2][CO4]	**[04M]**
2	What is Main Memory and what are the types in it? Explain in detail.		[L4][CO4]	**[12M]**
3	Categorize the semiconductor RAM in detail.		[L4][CO4]	**[12M]**
4	Classify in detail about ROM.		[L4][CO4]	**[12M]**
5	a	Define track and sector. Analyze the importance of auxiliary memory?	[L4][CO4]	**[06M]**
	b	Compare various types of Auxiliary memory.	[L2][CO4]	**[06M]**
6	a	Explain about hit and miss in the memory?	[L2][CO4]	**[04M]**
	b	Define Cache Memory? Explain in detail its mapping functions.	[L3][CO4]	**[08M]**
7	What is Virtual Memory? Discuss how paging helps in implementing virtual memory.		[L2][CO4]	**[12M]**
8	Describe the use of DMA controllers in a computer system with a neat block diagram.		[L2][CO4]	**[12M]**
9	Give detailed notes on DMA controllers and transfers with neat sketch.		[L4][CO4]	**[12M]**
10	a	Differentiate between RAM & ROM?	[L4][CO4]	**[06M]**
	b	Distinguish between SRAM & DRAM?	[L4][CO4]	**[06M]**

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UNIT –V

PIPELINIG & PARALLEL PROCESSORS

1		Categorize and discuss various forms of parallel processing based on Flynn's taxonomy with a neat sketch.	[L4][CO5]	**[12M]**
2	a	Describe the concept of Pipelining with clear example.	[L2][CO5]	**[08M]**
	b	Write the characteristics of Multiprocessor.	[L3][CO5]	**[04M]**
3	a	Sketch the arithmetic pipeline for floating point multiplication?	[L3][CO5]	**[06M]**
	b	Illustrate the instruction pipeline with neat timing diagram.	[L4][CO5]	**[06M]**
4		Define the hazards? Explain in detail about instruction hazards?	[L3][CO5]	**[12M]**
5		Describe the Interconnection Structures in detail.	[L3][CO5]	**[12M]**
6	a	Sketch 8×8 omega switching network and explain it.	[L3][CO5]	**[06M]**
	b	Express about crossbar switch with neat sketch?	[L2][CO5]	**[06M]**
7	a	What is multistage network? Appraise it with neat sketch.	[L5][CO5]	**[06M]**
	b	Write about hyper cube network with neat sketch?	[L3][CO5]	**[06M]**
8	a	Anticipate the conflicts in pipelining and describe about it.	[L6][CO5]	**[06M]**
	b	Construct 4-segment Instruction Pipeline and explain.	[L6][CO5]	**[06M]**
9		Implement three types multiprocessor system with neat sketch.	[L6][CO5]	**[12M]**
10		Illustrate the cache coherency.	[L4][CO5]	**[12M]**

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